THAT WHICH IS CLAIMED IS:

1. Method of controlling a cell of an EEPROM memory (1) having a floating gate transistor (Mlec), the method comprising at least a step of setting a state of the cell (1),

- characterized in that:

- the state setting step comprises applying simultaneously voltage pulses of opposite polarities respectively to the drain (DF, DS) and to the control gate (CG) of the floating gate transistor (Mlec);

- the pulses comprise:

- a first portion (11) having a slope greater than K* 8MegaVolts/s;

- a second portion (12) having a slope comprised between K* 1KiloVolts/s and K*1MegaVolts/s;

with K=1 when the pulse has a positive polarity, K=-1 when the pulse has a negative polarity.

2. Method according to claim 1, characterized in that the pulses further comprise a third portion (13) having substantially zero slope.

3. Method according to claim 2, characterized in that the pulses further comprise a fourth portion (14) having a slope less than K*16MegaVolts/s.

4. Method according to any one of the preceding claims, characterized in that at least one state setting step is a programming step, wherein:

- the voltage applied to the control gate is negative; and

- the voltage applied to the drain is positive.

5. Method according to any one of the preceding claims, characterized in that at least one state setting step is an erasing step, wherein:

- the voltage applied to the control gate is positive; and

- the voltage applied to the drain is negative.

6. Method according to any one of the preceding claims, characterized in that the voltages applied simultaneously to the control gate and to the drain have a same amplitude.

7. Method according to any one of the preceding claims, characterized in that:

- the transistor has a substrate (B);

- the method further comprises a step of applying the drain voltage on the substrate, at least during said state setting step of the cell.

8. Method according to claim 7, characterized in that:

- the polarities of the applied voltages are defined relative to a reference voltage;

- the substrate has a ground whose voltage is the reference voltage.

9. Method according to any one of the preceding claims, characterized in that the amplitudes of said applied voltages are less than 10 volts.

10. Method according to any one of the preceding claims, characterized in that the potential difference between the control gate and the drain is

comprised between 12 and 16 volts during the simultaneous application of the voltages.

11. Method according to any one of the preceding claims, characterized in that:

- the cell further presents a selection transistor (Msel), whose source (S) is connected to the drain (DF) of the floating gate transistor (Mlec);

- a voltage of less than 12 volts is applied to the gate of the selection transistor, optionally during the cell programming or erasing step.

12. Method according to claim 11, characterized in that the voltage applied to the drain of the selection transistor has the same polarity as the voltage applied to the drain of the floating gate transistor during said state setting step.

13. Electronic device:

- comprising at least one EEPROM memory cell (1) and one cell power supply;

- amenable for implementing the method according to any one of the preceding claims.

14. Electronic device according to claim 13, characterized in that:

- the electronic device is a made on a P-type substrate;

- the cell has a floating gate transistor made on the surface of a P-type well;

- the electronic device has an N-type isolation well separating the P-type well from the P-type substrate.